Reducing Power Consumption of an Embedded DSP Platform through the Clock-Gating Technique

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***Abstract*—The paper describes application of the clock-gating techniques, often used in ASIC designs, to the field of FPGA-based systems. The clock-gating techniques are used to reduce the total power of the system. To achieve this, we reduce clock power consumption of the system by switching-off the clock signal for the parts of system that are not used.**

The system presented in this paper is based on the main processor, extended with several reconfigurable accelerators. These accelerators extend the processor capabilities by several vector operations and can be reprogrammed in run-time. Clock gating, in our design, is used to switch the accelerators off when not used. As the accelerators can represent a major part of the system size, switching them off can significantly reduce the power consumption. We also propose the method for estimation of the reduction of power consumption that can be achieved using the clock-gating technique,

I. Introduction

With the increasing size and complexity of today's SoC systems, reduction of power consumption has become an important issue and an area of very active research. Clock gating (i.e. switching off the clock input of registers in cycles when they are not used) is one of techniques used in ASIC designs to reduce dynamic power. Current FPGA devices contain multiple networks for distribution of clock signal and, in principal, allow for use of the clock gating technique [1], [2].

In this paper, we present the results of power consumption measurements on design with and without clock gating technique on FPGA. The experiments were performed on *UTIA DSP platform* [3], which is a master-worker based multi-core architecture with MicroBlaze as master and a reprogrammable accelerators as worker. We also discus our proposed equation for power consumption reduction estimation through the clock gating.

The paper is organized as follows. In Section II, we shortly present the UTIA DSP platform and propose the implementation of the clock gating method for that platform. In Section III, a set of experiments is presented and results are discussed. In Section IV, the derivation of equation for estimating the power consumption reduction is presented. Finally, Section V concludes the work.

II. System description

The computing platform used in our work is based on the Xilinx MicroBlaze (MB) soft-processor (*http://www.xilinx.com*), which is a RISC architecture processor completely implemented in the FPGA fabric and on the *UTIA Basic Computing Elements* (BCE). The processor uses the BCE unit to accelerate computations and to off-load some tasks. The architecture is described in detail in [3].

Current FPGA devices do not support the power-off technique, that is, they do not allow to dynamically switch-off the power of the design part temporally not used. In our DSP platform, we have implemented clock gating of the BCE units to reduce their dynamic power consumption in the IDLE time.

To implement clock gating, we use an extra DCM block and BUFGCE dedicated only to BCE. The BUFGCE, which is used to enable or disable the BCE clocks, is controlled by the MB processor through the XPS_GPIO module connected to the PLB bus (Figure 1).

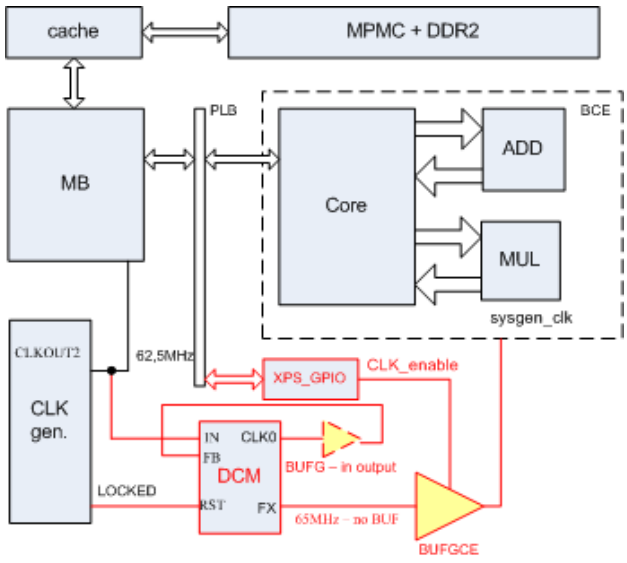

Fig. 1. System with clock gating.

III. Power consumption measurements

In this section, the power consumption measurements of system with one BCE unit are presented. The system consists of a single MicroBlaze processor with DDR2 controller, 2kB data and 2kB instruction cache, floating-point unit connected

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to the processor and RS232 interface. To that base system, a single BCE 1x4 unit is connected with the following functionality: *base* - vector copy, add and multiply; *DOT:* same operations as *base* + vector product and multiply-accumulate; *DOT4:* same operations as *DOT* + vector product.

Please note that the BCE versions (*base*, *DOT* and *DOT4*) differ in complexity of the dataflow unit, resulting in different BCE sizes. In all experiments, the MB processor is clocked at 62.5MHz and the BCE at 65MHz.

As the target platform, the Xilinx Spartan-3 Xtreme DSP board with Xilinx Spartan 3A DSP 1800 has been chosen. This board has the advantage that it is relatively easy to measure input current on all power sources (1.2V, 2.5V, 3.3V). The 1.2V power source is used exclusively as the internal supply voltage (VCC).

All measurements were performed using the Agilent MSO6034A Mixed Signal Oscilloscope (300MHz; 2GSa/s) with Agilent N2783A Current Probe (30A; 100MHz; 0.1V/A (10:1)). (*http://www.homeagilent.com*)

A. Power consumption of the system

The first power consumption measurement was done on a simple system with MB, DDR2, cache, RS232, both with and without BCE 1x4 unit. In these designs, clock gating is not implemented.

The following scenarios were used: 1. MB and BCE units are in IDLE state (no computation); 2. BCE computes vector addition (VADD); 3. BCE computes element-wise multiply (VMULT); 4. BCE computes multiply-accumulate operation (VMAC); 5. BCE computes vector product (VPROD); 6. BCE computes sum of vector products (VPROD_ S4).

The results of the system measurements with and without one BCE 1x4 are summarized in Table I. To identify the system state, the MB processor is running an infinite *while(1)* loop of a sequence of vector operations on 250 element data vectors. Each vector operation is initiated 256 times using the BCEs internal controller to stabilize the current consumption. Vector operations are run in the following pattern: 10,000x NOPs, VADD, VADD, VMULT, VPROD, VPROD_S4. The C program is compiled with -O2 optimization.

BCE 1x4	no BCE	with BCE		
Type	–	Base	DOT	DOT4
Op.	I [mA]	I [mA]	I [mA]	I [mA]
VADD	NA	434.0	466.5	477.0
VMUL	NA	431.0	464.0	474.0
VMAC	NA	NA	448.0	456.0
VPROD	NA	NA	472.0	493.0
VPROD4	NA	NA	NA	490.0
Idle	174.0	315.0	331.0	328.0
Size of the design				
DSP48As	8	24	24	24
RAMB16	10	38	38	38
Slices	3430	6766	8018	8413

TABLE I
POWER MEASUREMENTS OF THE BASE SYSTEM WITHOUT BCE AND OF THE SYSTEM WITH BCE 1X4 WITHOUT CLOCK GATING

As can be seen from Table I, the BCE 1x4 systems size and power consumption increased approximately twice. In the following paragraphs, we compare these results to the BCE 1x4 unit based system with clock gating.

B. Power consumption of a system with clock gating

These measurements were performed on a similar system as in previous case (MB, DDR2, 2x cache, RS232) with a BCE 1x4 unit (*base*, *DOT*, *DOT4*) with clock gating. The results are summarized in Table II.

Comparing the results to system without clock gating, we can see that the power consumption in idle mode is significantly reduced in IDLE mode (up to 30% of the overall system consumption). On the other hand, there is a slight increase (about 2.5%) in power consumption at computation state (VADD, VMUL etc.). This is in direct relation with the increase of the design size (about 2.7%).

1x4	BCE with clock gating		
	Base	DOT	DOT4
Op	I [mA]	I [mA]	I [mA]
VADD	435.0	472.0	489.0
VMUL	432.5	469.0	485.5
VMAC	NA	45.01	468.0
VPROD	NA	473.0	504.0
VPROD4	NA	NA	501.0
Idle	237.5	244.5	248.0
Size of the design			
DSP48As	24	24	24
RAMB16	38	38	38
Slices	6787	8183	8648

TABLE II
POWER MEASUREMENTS OF THE UTIA BCES 1X4 WITH CLOCK GATING

Similar results were obtained for other SIMD versions of the BCEs (i.e. BCE 1x1, 1x2 and 1x8). The reduction in power consumption at IDLE mode varies from 11.3% to 35% of overall system power consumption and the increase of power consumption in computing mode is up to 3.0%.

IV. ESTIMATION OF POWER REDUCTION

The system power estimation can be calculated by the Xilinx Power Analyzer (XPA) which provides detailed power analysis of post-implemented place-and-routed design or the Xilinx Power Estimator (XPE) can be used for power analysis at any time during the design cycle. (*http://www.xilinx.com/*)

Sometimes it is useful to estimate the power reduction with the use of clock-gating technique but XPA is not capable of doing this task in a simply way.

In this section we propose a way for estimation of power consumption reduction in our system with clock gating.

A. Derivation

As can be seen from Table III, the input current difference between BCE 1x4 base with clock gating and BCE 1x4 Dot with clock gating depends only on a number of Slices used by each system, because the number of DSP48 and RAMB16 blocks is same for both systems. The same holds for the

System	gating	Slices	DSP48	RAMB	I [mA]
no BCE	-	3430	8	10	174.0
1x2 base	No	5796	16	26	259.0
1x2 base	Yes	5680	16	26	221.0
1x2 Dot	No	6570	16	26	272.0
1x2 Dot	Yes	6412	16	26	223,5
1x2 Dot2	No	6474	16	26	263.5
1x2 Dot2	Yes	6758	16	26	219.5
1x4 base	No	6766	24	38	316.5
1x4 base	Yes	6787	24	38	236.5
1x4 Dot	No	8018	24	38	330.5
1x4 Dot	Yes	8183	24	38	243.5
1x4 Dot4	No	8413	24	38	327.5
1x4 Dot4	Yes	8648	24	38	245.0
1x8 base	No	9508	40	62	316.5
1x8 base	Yes	9225	40	62	236.5
1x8 Dot	No	11530	40	62	330.5
1x8 Dot	Yes	11843	40	62	243,5
1x8 Dot8	No	12371	40	62	451.0
1x8 Dot8	Yes	12208	40	62	298.5

TABLE III
SIZE AND POWER MEASUREMENTS OF DIFFERENT TYPES OF DESIGN

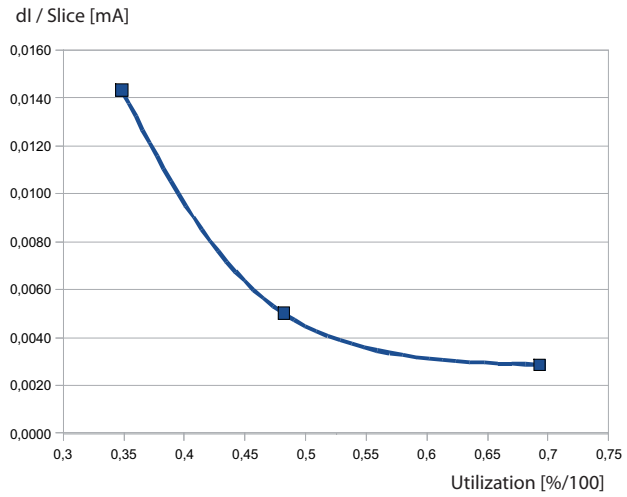

Fig. 2. Power reduction (current) on slices ($dI/Slice$) of BCE as a function of FPGA utilization.

BCE 1x2 or 1x8 systems. This characteristic came from same structure of these BCE units.

1) Current reduction per Slice: If we calculate difference in input current reduction of two BCE units with clock-gating, can we determine current reduction per Slice.

The difference in input current reduction (dI) 1x4 Dot with clock gating and 1x4 base with clock gating is:

$$dI = 243,5 - 236.5 = 7 \text{ mA}$$

Difference in size 1x4 Dot with clock gating and 1x4 base with clock gating is:

$$dS = 8183 - 6787 = 1396 \text{ (Slices)}$$

Using these figure, we get the raw estimate of current reduction per Slice (dI_{Slice}):

$$dI_{Slice} = 1396/7 \doteq 0.0050 \text{ mA}$$

System with clock-gating	Utilization [%]	dI on Slice dI_{Ss} [mA]
1x2 (base-Dot)	0.35	0.0143
1x4 (base-Dot)	0.48	0.0050
1x8 (base-Dot)	0.69	0.0029

TABLE IV
DEPENDENCY OF A SLICE POWER REDUCTION ON FPGA UTILIZATION

If we determine current reduction per Slice for BCE units 1x2, 1x4 and 1x8, we get figures quoted in Table IV. The interleaved dependency curve is shown in Figure 2.

It is evident from measured reduction per Slice (Table IV and Figure 2), that dI_{Slice} is non-linearly dependent on the ratio of FPGA utilization (for the given frequency).

We tried to approximate this data by equation (1), where k is a constant, S_{max} is the theoretical maximum size of BCE in % (with respect to the size of FPGA), S is the size of BCE in the FPGA (in %) and μ is minimal power reduction per slice.

$$dI_{Slice} = \left(\frac{1}{k} \times (S_{max} - S)^n + \mu\right) \; [mA] \qquad (1)$$

The equation (2) is the result of approximation for the given data.

$$dI_{Slice} = \left(\frac{1}{20} \times (0.86 - S)^4 + 0.0026\right) \; [mA] \qquad (2)$$

In the system, S is defined as $S = N_S/16640$, where N_S is number of Slices of the design and 16640 is the number of Slices in the Xilinx Spartan 3A DSP 1800 FPGA.

2) Current reduction per DSP48 and RAMB16: As we have estimate of power reduction on a slice, we continue by calculation of current reduction (dI_{Ss}) on all Slices (N_{Ss}) of BCE 1x4 base with clock gating:
$dI_{Ss} = dI_{Slice} \times N_{Ss} = 0.0050 \times (6787 - 3430) \doteq 16.83$mA
From the difference in input current reduction (dI) between systems 1x4 base and 1x4 base with clock gating($316.5 - 236.5 = 80mA$) it is possible to calculate input current reduction of DSPs and BRAMs:

$$dI_{DSP} + dI_{ram} = 80 - 16.8 \doteq 63.2\text{mA}$$

In the same way we get input current reduction per slice in systems 1x8 base and 1x8 Dot: $dI_{slice} \doteq 0.0029$mA, Input current reduction on all slices of 1x8 base with clock gating: $dI_{Ss} = 16.6$mA and power reduction of DSPs (dI_{DSP}) and BRAMs (dI_{RAM}) is:

$$dI_{DSP} + dI_{RAM} \doteq 125.6\text{mA}$$

From these calculations we get equations (3) and (4) for current reduction of DSPs and BRAMs.

$$63.17 = 16 \times dI_{DSP} + 28 \times dI_{RAM} \qquad (3)$$

$$125.4 = 32 \times dI_{DSP} + 52 \times dI_{RAM} \qquad (4)$$

By solving equations (3) and (4) it is possible to get the estimate of power reduction on a DSP and a BRAM for

BCE	Slices	D	R	I [mA]	dI_m [mA]	dI_{Ss} [mA]	Δ [mA]	%
1x1 b	1914	4	10	240.0	33.5	29.5	4.0	-11.8
1x1 D	2012	4	10	238.0	27.0	29.8	-2.8	10.5
1x2 b	2366	8	16	259.0	38.0	46.3	-8.3	21.9
1x2 D	3140	8	16	272.0	48.5	47.6	0.9	-1.9
1x2 D2	3044	8	16	263.5	44.0	47.5	-3.5	7.9
1x4 b	3336	16	28	316.5	80.0	78.9	1.1	-1.4
1x4 D	4588	16	28	330.5	87.0	79.8	7.2	-8.3
1x4 D4	4983	16	28	237.5	82.5	80.1	2.4	-3.0
1x8 b	6078	32	52	430.0	142.0	143.3	-1.3	0.9
1x8 D	8100	32	52	446.0	149.5	146.8	2.7	-1.8
1x8 D8	8941	32	52	451.0	152.5	148.7	3.8	-2.5
2x4 b	6112	32	56	436.0	144.5	144.3	0.2	-0.1
2x4 D	9011	32	56	458.5	167.0	149.8	17.2	-10.3
2x4 D4	9441	32	56	459.0	166.0	150.9	15.1	-9.1
1x4Fb	4695	18	28	320.0	75.0	86.9	-11.9	15.9
1x4FD	5991	18	28	320.0	79.0	88.1	-9.1	11.5
1x4FD4	6190	18	28	320.0	82.0	88.3	-6.3	7.7
2x4Fb	8796	36	56	439.0	157.0	163.5	-6.5	4.1
2x4FD	10608	36	56	461.0	174.0	168.1	5.9	-3.4
2x4FD4	10642	36	56	465.0	177.0	168.2	8.8	-5.0
2x4D4 +1x2D2	11016	40	72	538.0	205	187.0	18.0	-8.8

TABLE V
SIZE OF NON-GATED DESIGNS (SLICES, DSP48AS: D, RAMB16: R); MEASURED INPUT CURRENT (I); MEASURED CURRENT REDUCTION (dI_m) AND POWER ESTIMATION (dI_{Ss}) OF DIFFERENT DESIGNS (B = BASE, D = DOT, D2/4/8 = DOT2/4/8, FX = CORE X WITH FFT)

the BCE clocked at 65MHz, which can be expressed by the following equations:

$$dI_{DSP} = \frac{5659}{1600}\ mA;\ \ dI_{RAM} = \frac{47}{200}\ mA \tag{5}$$

Note that these values are valid only for 65MHz and for systems with the same characteristics.

3) Overall power reduction: We get equation for estimation the power reduction (dI) as a sum of power reduction on Slices, DSPs and BRAMs:

$$dI = dI_{Slice} \times N_{Ss} + dI_{DSP} \times N_{DSP} + dI_{RAM} \times N_{RAM}\ [mA] \tag{6}$$

B. Evaluation

The equation for estimation of power reduction was verified on several designs. It can be seen from Table V that equation (2) provides quite reliable power reduction estimate (dI_{Ss}). In column Δ is calculated variation between measured power reduction (dI_m) and calculated power reduction estimation (dI_{Ss}). In the last column (%) is the difference in percentage.

It is however necessary to interpret these figures properly: $\Delta = 4$mA on 33mA is 11.2% but $\Delta = 15$mA on 166mA represents only 9.1%. It is evident that the interpretation of this results is a non-trivial task.

C. Conclusion

Table V shows that our equation for current reduction estimation (6) is valid for all types of our system, even for its smaller (eg. 1x2) or larger (eg. 1x8) variants. It supports the assumption that the equation is valid also for different designs used for derivation of the equation. Power reduction on DSP48s and RAMB16s blocks is constant and does not depend on the FPGA utilization. The presented results holds only for one the FPGA Xilinx Spartan 3A DSP 1800 and the design running at 65MHz.

V. CONCLUSION AND FUTURE WORK

We have presented the implementation of the clock gating technique on the UTIA DSP platform. The reduction in power consumption has been demonstrated. All measurements have been performed on the Xilinx Spartan-3 Xtreame DSP board. The experiments show that for the system with one accelerator connected to MB, the clock gating technique gives the reduction in power consumption of up to 30% at IDLE state, while in computing mode, the power consumption increases up to 3.0% of the overall system consumption. The additional reduction in power consumption can be achieved using the area restriction method. This technique reduces the power consumption of the system up to 5.5%.

We have also proposed and validated a simple method for raw estimation of *reduction* of the BCE power consumption in IDLE state.

All results show that the clock gating technique leads to power consumption reduction of the overall system and that clock gating is useful technique for power consumption reduction of temporarily unused parts of the system, such as accelerators etc.

The future work will include the measurements of power consumption of a system clocked at different frequencies and measurements on different Spartan 3A DSP FPGAs.

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